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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 10/076,374

Filing Date: February 15, 2002

Appellant(s): VAN DER SCHAAR, MIHAELA

Robert M. McDermott, Esq.  
Reg. No. 41,508  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 1/11/07 appealing from the Office action  
mailed 8/25/06.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

6,956,972	Wu et al.	10-2005
6,798,364	Chen et al.	9-2004

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6,456,744	Lafe	9-2002
WO98/37700	Monro	8-1998

### **(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

1. Claims 38-40 are rejected under 35 U.S.C. 101 because the claims do not meet the 35 U.S.C. 101 requirements (the claims have improper language regarding the computer readable medium). Please see the USPTO "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility" in the Official Gazette notice of 22 November 2005, Annex IV, page 53. The examiner further suggests changing "includes" in line 1 of claim 38 to "encoded with" to meet the 101 Interim Guidelines (page 53, lines 7-11).
2. Claims 21-27, 29-32, 35-36, 38, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (6956972), (hereinafter referred to as "Wu") in view of Chen et al. (6798364), (hereinafter referred to as "Chen").

Regarding claims 21, 29-30, and 38, Wu discloses an apparatus that relates to motion compensation based video coding (Wu: column 1, lines 13-16). This apparatus comprises "receiving a plurality of transform blocks" (Wu: figure 9), "converting each of the blocks into bit-plane encodings" (Wu: figure 9, wherein the bit-plane VLC performs converting), and "transmitting each encodings of the blocks in order" (Wu: column 4, lines 59-67). However, this apparatus lacks storing the bit-plane encodings prior to converting another block

as claimed. Chen teaches that prior art computing systems introduce mispredicted branches which cause processor slowdown (Chen: column 1, lines 45-53). To help alleviate this problem, Chen discloses "storing each of the bit-plane encodings in a memory" (Chen: column 5, lines 33-36). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to take the apparatus disclosed by Wu and add the storage taught by Chen in order to obtain an apparatus that operates more efficiently by preventing processor slowdown.

Regarding claims 22 and 31, although not disclosed, it would have been obvious to store the bit-plane from MSB to LSB (Official Notice). Doing so would have been obvious in order to easily find a desired part of the stream.

Regarding claims 23, 32, and 40, although not disclosed, it would have been obvious for the encoding to include run length encoding (Official Notice). Doing so would have been obvious in order to compress the data for easier transmission.

Regarding claim 24, Chen discloses "storing each bit-plane encoding includes storing the encoding for each subsequently received block in locations following the encoding of a prior received block" (Chen: column 5, lines 33-36, wherein two bit planes are sequentially stored in memory).

Regarding claim 25, although not disclosed, it would have been obvious to discard each block after the transform process (Official Notice). Doing so would have been obvious in order avoid sending redundant data over a network.

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Regarding claims 26 and 35, Chen discloses "each transform blocks corresponds to a fine granular scalability encoding" (Chen: column 1, lines 30-31).

Regarding claims 27 and 36, Wu discloses "the transform blocks correspond to a DCT" (Wu: figure 9).

3. Claims 28 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (6956972), (hereinafter referred to as "Wu") in view of Chen et al. (6798364), (hereinafter referred to as "Chen") in further view of Lafe (6456744).

Regarding claims 28 and 37, note the examiners rejection for claim 21, and in addition, claims 28 and 37 differ from claim 21 in that claims 28 and 37 further require identifying the maximum transform coefficient. Lafe teaches that there is a need for fast and effective compression (Lafe: column 1, lines 35-38). To help alleviate this need, Lafe discloses "identifying a maximum transform coefficient within the block and determining the encodings for the block based on the coefficient" (Lafe: column 17, lines 26-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the processing taught by Lafe in order to obtain an apparatus that provides fast and effective compression.

4. Claims 33-34 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (6956972), (hereinafter referred to as "Wu") in view of Chen et al. (6798364), (hereinafter referred to as "Chen") in further view of Monro (WO 98/37700).

Regarding claims 33-34 and 39, note the examiners rejection for claim 21, and in addition, claims 33-34 and 39 differ from claim 21 in that claims 33-34 and 39 further require storing the bit plane encodings in a third location which is between the first two locations. Monro teaches storing data in an interleaved format, or between two locations (Monro: figures 2-3). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the storage taught by Monro in order to obtain an apparatus that provides fast and effective memory access.

**(10) Response to Argument**

- i. On page 5, appellant argues that the Office Action asserts that a claim to a computer readable medium that includes computer program code must specifically use the term “encoded with” instead of “includes” to overcome the 101 rejection.

The Office Action was not asserting the specific term “encoded with” must be used. Rather, the term “encoded with” was offered as a suggestion to the appellant as acceptable language to place the claim in statutory form. Please note the MPEP 2106.01, Section 1 titled “Functional Descriptive Material”. Section 1 describes computer programs claimed as computer listings per se, i.e., the descriptions or expressions of the programs, are not physical things, and are not statutory processes. In contrast, a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships and is thus statutory. Thus, the term “encoded with” was offered as a suggestion to the appellant to place the claim in statutory form.

ii. On page 6, appellant argues that Wu and Chen fail to teach storing each of the plurality of bit-plane encodings in a sequential bit-plane order of memory prior to converting another of the transform blocks. The appellant further argues that the Office Action fails to address storing the encoding of each block's bit-plane encoding prior to converting another block.

Storing the encoding of each block's bit-plane encoding prior to converting another block is not found in the claim. What is found in the claim is storing each of the bit-plane encodings in a sequential bit-plane order of memory prior to converting another of the blocks. See for example Wu figure 9. The video is input into a frame separator 206 and then to a DCT 208 which performs the conversion one block at a time. After the DCT performs the conversion on a single block, the block is sent to a quantizer 210, then a frame memory 222, and then a plurality of bit-plane coders 226(1), 226(n-1), and 226(n). Wu further discloses in column 9, lines 39-50, the 64 absolute values of the block are arranged in a zigzag order into a one-dimensional array and stored in memory 222, thus indicating the data is processed block-by-block and not an entire frame at a time. Since the data is processed block-by-block, another conversion would not take place until the current block is output to memory. Since Wu did not clearly show the storing in a sequential bit-plane order of memory, the examiner relied upon Chen to show this limitation. Chen discloses in column 5, lines 22-37, that a bit-plane is extracted from a source in multiple passes. At the end of each pass, the destination buffer is shifted and the selected bits of the current pass are extracted into the right-most position of the buffer, thus indicating the storing of the bit-plane

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encodings in a sequential bit-plane order. Further, since the data is processed in passes, the next pass, or conversion, will not begin until the current pass is stored in memory. Therefore the combination, taken as a whole, teach storing each of the bit-plane encodings in a sequential bit-plane order of memory prior to converting another block.

iii. On page 7, appellant argues that Wu and Chen fail to teach storing the bit-plane encoding for each subsequently received transform block in memory locations following the stored bit-plane encoding of a prior received transform block.

As indicated in the above argument, Wu illustrates in figure 9 and column 9, lines 39-50, processing the input video data on a block-by-block basis. Since Wu did not clearly show storing the blocks in memory locations following the stored current location, the examiner relied upon Chen to show this limitation. Chen discloses in column 5, lines 32, that a bit-plane is extracted in multiple passes. At the end of each pass, the destination buffer is shifted and the selected bits of the current pass are extracted into the right-most positions of the buffer. Since the buffer is continually filled to the right-most position, each subsequently received block of data is stored in a location following the previously stored block of data. Therefore the combination, taken as a whole, teach storing the bit-plane encoding for each subsequently received transform block in memory locations following the stored bit-plane encoding of a prior received transform block

**(11) Related Proceeding(s) Appendix**

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No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

**(12) Evidence Appendix**

No evidence has been submitted by appellant.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Dave Czekaj



Conferees:

Mehrdad Dastouri, SPE

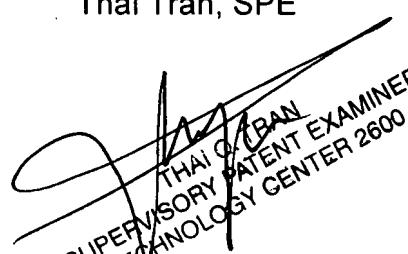
Thai Tran, SPE



MEHRDAD DASTOURI

SUPERVISORY PATENT EXAMINER

TC 2600



THAI TRAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600